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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/735,054

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EXAMINER

COLEMAN, ERIC

ART UNIT

PAPER NUMBER

2183

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/735,054

Applicant(s)

EICHENBERGER ET AL.

Examiner

Eric Coleman

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 May 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 12-15 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claimed program product is not tangibly embodied in a manner so as to be executable. The computer program product as claimed is a medium having computer readable code. This medium has not been limited to a tangible medium (such as a storage or memory). Therefore the claims are directed toward and abstract idea and does not fall into one of the categories of invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
4. Claim 1(line 6) contains the language "creating ad new register"; claim 12(lines 10-22) contain the language "create a new register" ;claim 16 (line 7) contains the language (for creating a new register).The claims that depend from these independent claims respectively contain the above language. As to these limitations it is unclear

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what operation is being claimed. Is a new register being fabricated such that the system is being rebuilt or is a current register being a reassigned.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3,10-19,21,22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kunimatsu et al. (patent No. 6,938,149).

7. Kunimatsu taught the invention as claimed including a data processing ("DP") system comprising (as per claims 1,12):

a) Introducing a name level instruction (register rename instruction) for at least one of a named architected register in a processor (e.g., see fig. 1,3 and col. 3, lines 50-61 and col.4, lines 12-56 and col. 5, lines 17-30);

b) Allowing a programmer to change the current name level of a register name via said name level instruction (e.g., see figs. 1,3 and col. 4, lines 12-56 and col. 5, lines 17-30)[the rename instruction is accessible for programming by a programmer of the system performing renaming of registers];

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c) Renaming a register to a new name level and (as the claims is understood) creating a new register (e.g., see col. 4, lines 5-56);

d) Providing a plurality of additional computer registers (register file 6) (e.g., see col. 4, lines 44-61).

8. As to the further limitations of claim 12, Kunumatsu taught program code for causing the computer to perform the above discussed features (e.g., see col. 3, lines 50-60 and col. 4 lines 5-56)

9. As per claims 2,3,13,21Kunimatsu taught the name level instruction is used for hardware renaming (e.g., see col. 6, lines 5-9) and maintains a pointer for a current physical register for a corresponding architected register (e.g., see fig. 5 and col. 4, lines 45-60 and col. 4, lines 23-56).

10. As to claims10,14 Kunimatsu taught the name level instruction (rename instruction) provides for the facilitation of architectural features which overload the architected register namespace reducing the overhead of register management (e.g., see col. 1, line 26-col. 2, line 48).

11. As to claims 11,15,22, Kunimatsu taught the name level instruction (rename instruction) provides for additional computer registers without changing the instruction format of the computer (e.g., see fig. 3 and col. 4, lines 5-56).

12. As per claim 16 Kunimatsu taught a memory (1); at least one execution unit(7) in cooperation with instructions and comprising circuitry to manage data in a register (e.g., see fig. 1); said data register further comprising a plurality of registers (6); and a register renaming mechanism (4) coupled to a stack or register names and responsive to a

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name level instruction for creating a new register with an internal name and a new name level by changing a current name level of a register (e.g., see col. 4, lines 5-56).

13. As per claim 17, 18 Kunimatsu taught at least one of the registers is a physical register and at least one register is an architected register (e.g., see fig. 5).

14. As per claim 19, Kunimatsu taught the new register is an architected register (e.g., see col. 4, lines 44-67 and col. 5 lines 17-27).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claims 4-9 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kunimatsu et al. (patent No. 6,938,149).

17. Kunimatsu taught (claims 4-9) a system with a renaming instruction for providing selective correspondence between logical and physical register. Kunimatsu taught the system comprised register file which outputs to arithmetic logical unit and instruction memory within the element that comprises fetch unit and decode unit. (e.g., see fig. 1). Kunimatsu also taught logical and physical registers organized sequentially into plural bundles for during the execution of the renaming instruction (e.g., see fig. 5 and col. 4, lines 45-56). Therefore one of ordinary skill would have been motivated to implement the register bundles as register stacks and effectively cache the register data in bundles

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and this memory would have been a special purpose memory for used by the renaming instruction. Also since when all the available registers were in use and the renaming instruction was to be executed one of ordinary skill would have been motivated to use the main memory to store register data for freeing additional registers for use by the rename register and in the case the a register was already spilled to main memory when a rename instruction was executed one of ordinary skill would have been motivated to use the main memory to retrieve register data. Also as well known in the art at the time of the claimed invention the cache and storage would have been implemented as a memory hierarchy (e.g., see fig. 1).

18. As per claim 20, Kunimatsu taught a instruction processor that performed renaming of registers as discussed above and including an instruction pipeline (e.g., see fig. 1). One of ordinary skill would have been motivated to incorporate a backing store in the system at least maintain results of processing and control data so that data is not lost when adverse situations are encountered such as interrupts and power loss as was well known in the art at the time of the claimed invention.

Response to Arguments

19. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McLeod (patent No. 6,090,156) disclosed a system for local context spilling for graph coloring register allocators (e.g., see abstract).

Lin (patent No. 6,631,452) disclosed a register stack engine having speculative load/store modes (e.g., see abstract).


Brauch (patent No. 6,526,572) disclosed a mechanism for software renaming and load speculation in an optimizer (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC



ERIC COLEMAN
PRIMARY EXAMINER